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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/751,803	12/29/2000	Wolfgang Roesner	AUS920000227US1	5327

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EXAMINER	
STEVENS, THOMAS H	

ART UNIT	PAPER NUMBER
2123	7

DATE MAILED: 05/06/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No. 09/751,803	Applicant(s) ROESNER ET AL.	
	Examiner Thomas H. Stevens	Art Unit 2123	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *29 December 2000 & 10 October 2001*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-12* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-12* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *29 December 2000* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *(5)10/01/02*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 5-12 were added prior to prosecution.

2. Claims 1-12 were reviewed for prosecution.

Claim Interpretation

3. Office personnel are to give claims their **"broadest reasonable interpretation"** in light of the supporting disclosure. *In re Morris,* 127 F.3d 1048, 1054-55, 44 USPQ2d 1023, 1027-28 (Fed. Cir. 1997). Limitations appearing in the specification but not recited in the claim are not read into the claim. *In re Prater,* 415 F.2d 1393, 1404-05, 162 USPQ 541, 550-551(CCPA 1969). See *also *In re Zletz,* 893 F.2d 319, 321-22, 13 USPQ2d 1320, 1322(Fed. Cir. 1989) ("During patent examination the pending claims must be interpreted as broadly as their terms reasonably allow") .... The reason is simply that during patent prosecution when claims can be amended, ambiguities should be recognized, scope and breadth of language explored, and clarification imposed .... An essential purpose of patent examination is to fashion claims that are precise, clear, correct, and unambiguous. Only in this way can uncertainties of claim scope be removed, as much as possible, during the administrative process. **The examiner interprets an override signal as the signal response of the override circuit.**

Claim Rejections - 35 USC § 112

4. The following is a quotation of the first paragraph of 35 U.S.C. 112:

The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

5. Claims 1-12 are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the enablement requirement. The claims contains subject matter which was not described in the specification in such a way as to enable one skilled in the art to which it pertains, or with which it is most nearly connected, to make and/or use the invention. These claims are divorced from the teachings of how the signal is overridden during simulation.

explain

6. The following is a quotation of the second paragraph of 35 U.S.C. 112:

The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter, which the applicant regards as his invention.

7. Regarding claim 1,3,5, 7 and 9 the word "means" is recited. However, since no function is specified by the word(s) preceding "means," it is impossible to determine the equivalents of the element, as required by 35 U.S.C. 112, sixth paragraph. See *Ex parte Klumb*, 159 USPQ 694 (Bd. App. 1967).

8. Furthermore, claims 1-12 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention because the claims don't state what is doing the override and more specifically how. Additionally, the claim does not recite the type of signal or its end result.

Claim Rejections - 35 USC § 102

9. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

10. Claims 1-12 are rejected under 35 U.S.C. 102(b) as being anticipated by Swaboda et al. (U.S. Patent 5,805,792 (1998)).

Swaboda et al. teaches an electronic device having addressable storage elements and a bus so that the storage elements are accessible via the bus, and address register connected to the bus.

need to specifically refer to where reference teaches

Claim 1: A method for overriding a signal during model simulation (column 2, line 65 and column 26, lines 5-26) said method comprising: instantiating an override signal port for delivering an override signal from an instrumentation entity to a signal selection means, wherein said signal selection means selects between said signal and said override signal; declaring a signal override during model simulation; and in response to said declared signal override, selecting said override signal utilizing said signal selection means.

Claim 2: The method of claim 1, wherein said declaring step further comprises instantiating an override enable port for delivering an override enable signal (column 2, line 65 and column 26, lines 5-26).

Claim 3: The method of claim 2, further comprising delivering said override enable signal from said override enable port to said signal selection means (column 2, line 65 and column 26, lines 5-26).

Claim 4: The method of claim 2, further comprising: instantiating a latch that stores an override disable bit; and combining said override disable bit with said override enable signal within a logic gate to produce a combined selection signal that controls said

signal selection means(column 2, line 65 and column 26, lines 5-26).

Claim 5: A system for overriding a signal during model simulation, said system comprising: processing means for instantiating an override signal port for delivering an override signal from an instrumentation entity to a signal selection means, wherein said signal selection means selects between said signal and said override signal; processing means for declaring a signal override during model simulation; and processing means responsive to said declared signal override, for selecting said override signal utilizing said signal selection means(column 2, line 65 and column 26, lines 5-26).

Claim 6: The system of claim 5, wherein said processing means for declaring a signal override further comprises processing means for instantiating an override enable port for delivering an override enable signal (column 2, line 65 and column 26, lines 5-26).

Claim 7: The system of claim 6, further comprising processing means for delivering said override enable signal from said override enable port to said signal selection means (column 2, line 65 and column 26, lines 5-26).

Claim 8: The system of claim 6, further comprising: processing means for instantiating a latch that stores an override disable bit; and processing means for combining said override disable bit with said override enable signal within a logic gate to produce a combined selection signal that controls said signal selection means (column 2, line 65 and column 26, lines 5-26).

Claim 9: A computer program product for overriding a signal during model simulation, said computer program product comprising: processing means for instantiating an override signal port for delivering an override signal from an instrumentation entity to a signal selection means, wherein said signal selection means selects between said signal and said override signal; instruction means for declaring a signal override during model simulation; and instruction means responsive to said declared signal override, for selecting said override signal utilizing said signal selection means (column 2, line 65 and column 26, lines 5-26).

Claim 10: The computer program product of claim 9, wherein said instruction means for declaring a signal override further comprises instruction means for instantiating an override enable port for

delivering an override enable signal (column 2, line 65 and column 26, lines 5-26).

Claim 11: The computer program product of claim 10, further comprising instruction means for delivering said override enable signal from said override enable port to said signal selection means (column 2, line 65 and column 26, lines 5-26).

Claim 12: The computer program product of claim 10, further comprising: instruction means for instantiating a latch that stores an override disable bit; and instruction means for combining said override disable bit with said override enable signal within a logic gate to produce a combined selection signal that controls said signal selection means (column 2, line 65 and column 26, lines 5-26).

Correspondence Information

11. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Tom Stevens whose telephone number is (703) 305-0365, Monday-Friday (8:30 am- 5:30 pm) or contact Supervisor Mr. Kevin Teska at (703) 305-9704. The fax number for the group is 703-872-9306.

Any inquires of general nature or relating to the status of this application should be directed to the Group receptionist whose phone number is (703) 305-3900.

April 16, 2004

THS

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